83. (As Filed) The device of claim 66, wherein said second conductive layer pattern comprises polysilicon.

84. (As Filed) The device of claim 66, wherein said second insulating layer comprises a second oxide layer.

85. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a photoresist process.

86. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a wet etch process.

87. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a dry etch process.

88. (Previously Once Amended) The device of claim 66, wherein said second plurality of contact holes are filled by a CVD process.

REMARKS

Claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88 were pending in this application. Claims 1, 5, 6, 10, 12, 15, 17, 20, 23, 27, 30, 31, 32, 34, 36, 39, 41, 64, 65 and 66 have been amended. No other claims have been either amended, added or canceled. Hence, claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88 remain pending. Reconsideration of the subject application as amended is respectfully requested.

Claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over applicant's admitted prior art [AAPA] (as depicted in Figs. 1A and 1B of U.S. Patent No. 5,683,938) in view of

Gutierrez (U.S. Patent No. 5,069,749) taken together with Wolf (Textbook Chapter 4 Entitled "MULTILEVEL-INTERCONNECT TECHNOLOGY"). Applicant amends each of the pending independent claims, and respectfully traverses the rejection in light of the claims as amended.

As amended, Applicant's claim 1 includes, *inter alia*, forming contact holes that have a tapered upper portion, wherein the tapered upper portion is distinguishable from a substantially vertical lower portion. This is in stark contrast to the untapered hole taught and illustrated by Wolf at Fig. 4-43(a). Office Action of 3/14/2002 at pg. 4. The Office Action notes that the "real world" picture included as Fig. 4-43(b) shows that a vertical hole is only substantially vertical, while exhibiting some degree of taper. Id. Based on this and a broad reading of claim 1, it is asserted that prior to the amendment, claim 1 "read on the inherent taper of a vertical wall via expected as is shown in Fig. 4-43(b) of Wolf." Id. As amended, claim 1 does not read on Fig. 4-43(b), and for at least this reason the rejection is overcome and the claim is in condition for allowance.

Further, independent claims 1, 5, 6, 10, 12, 15, 17, 20, 23, 27, 30, 31, 32, 34, 36, 39, 41, 64, 65, and 66 have each been amended to include limitations not illustrated by Fig. 4-43(b). For at least this reason, the rejection of the claims is overcome and the claims are in condition for allowance. Further, all other claims depend from an allowable independent claim, and are thus also in condition for allowance for at least this reason.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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1. A method for filling contact holes with metal by two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively the first plurality of contact holes having a tapered upper portion, wherein the tapered upper portion is distinguishable from a substantially vertical lower portion;

filling a first metal layer into the first plurality of contact holes, entirely, the first metal layer being grown over and extending slightly beyond said first plurality of contact holes;

G1

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern respectively.

2. A method according to claim 1, wherein the first metal layer and subsequently the second metal layer are formed by chemical vapor deposition method.

cont.

3. A method according to claim 1, wherein the filling a second metal layer **[filled in each of]** fills the second plurality of **[contacts]** contact holes **[has]** to a substantially equal depth.

4. A method according to claim 1, wherein the first and second metal layers are selective tungsten layers, respectively, and the first and second plurality of contact holes are filled with the first and second metal layers of the selected tungsten layers, respectively.

5. A method for filling contact holes with metal by a two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

G1 cont.

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively the first plurality of contact holes having a tapered upper portion and a substantially vertical lower portion;

filling a first metal layer into entire first plurality of contact holes by one single step, the first metal layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern respectively.

6. A method of forming a substrate with contact holes, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

G1 Cont.

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, the first plurality of contact holes having a tapered upper portion, wherein a taper angle of the tapered upper portion is greater than a taper angle of the lower portion;

forming a first conductive material layer into the first plurality of contact holes, entirely, the first conductive material layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern, respectively; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern, respectively.

7. A method according to claim 6, wherein the first conductive material layer and subsequently the second conductive material layer are formed by a chemical vapor deposition process.

8. A method according to claim 6, wherein the forming a second conductive material layer fills the second plurality of contact holes to a substantially equal depth.

9. A method according to claim 6, wherein the first and second conductive material layers comprise first and second tungsten layers, respectively, and the first and second plurality of contact holes are filled with the first and second tungsten layers, respectively.

G1 Cont.

10. A method of forming a substrate with contact holes, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, the first plurality of contact holes having a tapered upper portion, the tapered upper portion being distinguishable from a substantially vertical lower portion;

forming a first conductive material layer into entire first plurality of contact holes in a continuous step, the first conductive material layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern, respectively; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern, respectively.

G1 Cont.

11. A method according to claim 10, wherein said steps of forming said first and said second conductive material layers comprise filling said first and said second plurality of contact holes, respectively.

12. A method of forming a substrate with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the junction layer;

forming a first contact hole of substantially equal depth to other contact holes in the first insulating layer by removing a portion of the first insulating layer to expose said junction layer, the first contact hole having a tapered upper portion, wherein a taper angle of the tapered upper portion deviates from a taper angle of the lower portion;

forming a first conductive material layer into the first contact hole, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first contact hole;

forming a second contact hole by removing portions of said second insulating layer to expose the first conductive material layer; and

forming a second conductive material layer into said second contact hole to contact the first conductive material layer.

13. A method as in claim 12, further comprising:

forming a third contact hole by removing portions of the second insulating layer to expose the conductive layer pattern; and

forming the second conductive material layer into the third contact hole to contact the conductive layer pattern.

G1 cont.

14. A method as in claim 12, wherein said first and said second conductive material layers comprise a metal.

15. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a silicon substrate;

forming an oxide layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said gate electrode, the first

plurality of contact holes having a tapered upper portion, wherein the tapered upper portion is distinguishable from the relatively untapered lower portion;

filling a first conductive material layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

filling a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

G1 cont.

16. A method as in claim 15, wherein said first and second conductive material layers comprise first and second metal layers.

17. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive material layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern, wherein a thickness of the first insulating layer is substantially uniform;

forming a first contact hole by removing a portion of the first insulating layer to expose said first conductive layer pattern, the first contact hole having a tapered

upper portion, wherein the tapered upper portion is distinguishable from a substantially vertical lower portion;

forming a first conductive material layer into the first contact hole, filling said first contact hole entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first conductive material layer;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

forming a second conductive material layer into said second and third contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

G1 cont.

18. A method as in claim 17, wherein said first conductive layer pattern comprises a gate electrode.

19. A method as in claim 17, wherein said first and second conductive material layers comprise first and second metal layers.

20. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the first conductive layer pattern;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said first conductive layer pattern, respectively, the first plurality of contact holes having a tapered upper portion, wherein the tapered upper portion includes a taper angle greater than a relatively vertical lower portion;

filling a first conductive material layer into the first plurality of contact holes, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

filling a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

G1 cont.

21. A method as in claim 20, wherein said first and second conductive material layers comprise first and second metal layers.

22. A method as in claim 20, wherein said first conductive layer pattern comprises a gate electrode.

23. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, and first and second regions on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and said first and said second regions;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said first and second regions, the first plurality of contact holes having a tapered upper portion, wherein the tapered upper portion includes a taper angle greater than a relatively vertical lower portion;

forming a first conductive material layer into, and filling entirely, the first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first conductive material layer;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

G1 cont.

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

24. A method as in claim 23, wherein said first region comprises a junction layer.

25. A method as in claim 23, wherein said second region comprises a gate electrode.

26. A method as in claim 23, wherein said first and second conductive material layers comprise first and second metal layers.

27. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, wherein said first plurality of contact holes have an upper portion and a lower portion, said upper portion exhibiting a first taper angle greater than a second taper angle exhibited by said lower portion;

forming a first conductive material layer into the first plurality of contact holes, entirely;

G1 cont.

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

28. A method as in claim 27, wherein said first and second conductive material layers comprise first and second metal layers.

30. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the junction layer;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer, the first plurality of contact holes having a tapered upper portion, wherein the tapered upper portion exhibits a taper angle greater than a taper angle of a lower portion;

forming a first metal layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

G1 Cont.

31. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the gate electrode;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said gate electrode, the first

plurality of contact holes having a tapered upper portion, wherein the tapered upper portion is distinguishable from a substantially vertical lower portion;

filling a first metal layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

32. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern, wherein a thickness of the first insulating layer is substantially uniform;

forming a first contact hole by removing a portion of the first insulating layer to expose said first conductive layer pattern, the first contact hole having a tapered upper portion, wherein the tapered upper portion is distinguishable from a substantially vertical lower portion;

forming a first metal layer into the first plurality of contact hole, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

G1 cont.

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first contact hole;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose the first metal layer and the second conductive layer pattern, respectively; and

forming a second metal layer into said second and third contact holes to contact the first metal layer and the second conductive layer pattern, respectively.

33. A method as in claim 32, wherein said first conductive layer pattern comprises a gate electrode.

34. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer and first conductive layer pattern on said substrate;

G1 cont.

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the first conductive layer pattern;

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said first conductive layer pattern, respectively, the first plurality of contact holes having a tapered upper portion, wherein the tapered upper portion is distinguishable from a substantially vertical lower portion;

forming a first metal layer into the first plurality of contact holes, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the second conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the second conductive layer pattern, respectively.

35. A method as in claim 34, wherein said first conductive layer pattern comprises a gate electrode.

36. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer, and first and second regions on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the first region and the second region;

G1 cont.

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said first and said second region, respectively, the first plurality of contact holes having a tapered upper portion and a substantially vertical lower portion;

forming a first metal layer into the first plurality of contact holes, to fill said first plurality of contact holes entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

37. A method as in claim 36, wherein said first region comprises a junction layer.

38. A method as in claim 36, wherein said second region comprises a gate electrode.

39. A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

G1 cont.

forming a first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, wherein said first plurality of contact holes have a tapered upper portion, and wherein a taper angle of the tapered upper portion is greater than a taper angle of a lower portion;

forming a first metal layer into the first plurality of contact holes, to fill said first plurality of contact holes entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming a second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

41. A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive material layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern, wherein a thickness of the first insulating layer is substantially uniform;

forming a first contact hole by removing portions of the first insulating layer to expose said first conductive layer pattern, wherein said first contact hole has an upper portion and a lower portion, said upper portion tapered at an angle greater than said lower portion;

G1 cont.

forming a first conductive material layer into the first contact hole, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first contact hole;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

forming a second conductive material layer into said second and said third contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

42. The method of claim 41, wherein said first conductive material layer comprises a metal.

43. The method of claim 42, wherein said metal comprises tungsten.

45. The method of claim 41, wherein said first conductive layer pattern comprises a gate electrode.

46. The method of claim 41, wherein said first conductive layer pattern comprises a gate electrode overlying a gate oxide.

47. The method of claim 41, wherein said forming an oxide layer and a first conductive layer pattern further comprises forming a junction layer.

G1 cont.

48. The method of claim 41, wherein said junction layer comprises a N+ junction.

49. The method of claim 41, wherein said junction layer comprises a P+ junction.

50. The method of claim 41, wherein said first conductive layer pattern comprises polysilicon.

51. The method of claim 41, wherein said first insulating layer comprises a first oxide layer.

52. The method of claim 41, wherein said step of forming said first contact hole comprises a photoresist process.

53. The method of claim 41, wherein said step of forming said first contact hole comprises a wet etch process.

54. The method of claim 41, wherein said step of forming said first contact hole comprises a dry etch process.

55. The method of claim 47, wherein said step of forming said first contact hole further exposes said junction layer.

56. The method of claim 41, wherein said first contact hole has a tapered upper portion.

G1 cont.

57. The method of claim 41, wherein said step of forming said first conductive material layer comprises a CVD process.

58. The method of claim 41, wherein said second conductive layer pattern comprises polysilicon.

59. The method of claim 41, wherein said second insulating layer comprises a second oxide layer.

60. The method of claim 41, wherein said step of forming said second and said third contact holes comprises a photoresist process.

61. The method of claim 41, wherein said step of forming said second and said third contact holes comprises a wet etch process.

62. The method of claim 41, wherein said step of forming said second and said third contact holes comprises a dry etch process.

63. The method of claim 41, wherein said step of forming said second conductive material layer comprises a CVD process.

64. A semiconductor device comprising:

a semiconductor substrate having an oxide layer, a junction layer and a gate electrode;

a first insulating layer overlying portions of said oxide layer, said junction layer and said gate electrode, said first insulating layer having a first plurality of contact holes of substantially equal depth over said junction layer and said gate electrode, said first plurality of contact holes having a tapered upper portion and a substantially vertical lower portion;

a first metal layer filling said first plurality of contact holes so that said first metal layer is in contact with said junction layer and said gate electrode;

a conductive layer pattern on said first insulating layer spaced apart from said first metal layer;

a second insulating layer overlying portions of said conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first metal layer and said conductive layer pattern; and

a second metal layer filling said second plurality of contact holes, said second metal layer in contact with said first metal layer and said conductive layer pattern.

65. A semiconductor device comprising:

a semiconductor substrate having an oxide layer, a junction layer and a gate electrode;

a first insulating layer overlying portions of said oxide layer, said junction layer and said gate electrode, said first insulating layer having a first plurality of contact holes of substantially equal depth over said junction layer and said gate electrode, said first plurality of contact holes having a tapered upper portion, wherein the tapered upper portion is distinguishable from a substantially vertical lower portion;

a first conductive material layer filling said first plurality of contact holes so that said first conductive material layer is in contact with said junction layer and said gate electrode;

a conductive layer pattern on said first insulating layer spaced apart from said first conductive material layer;

a second insulating layer overlying portions of said conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first conductive material layer and said conductive layer pattern; and

a second conductive material layer filling said second plurality of contact holes, said second conductive material layer in contact with said first conductive material layer and said conductive layer pattern.

G1 cont.

66. A semiconductor device comprising:

a semiconductor substrate having an oxide layer and a first conductive layer pattern;

a first insulating layer overlying portions of said oxide layer and said first conductive layer pattern, said first insulating layer having a first plurality of contact holes of substantially equal depth over said first conductive layer pattern, wherein said first plurality of contact holes have a tapered upper portion, wherein the tapered upper portion is distinguishable from a substantially vertical lower portion;

a first conductive material layer filling said first plurality of contact holes so that said first conductive material layer is in contact with said first conductive layer pattern;

a second conductive layer pattern on said first insulating layer spaced apart from said first conductive material layer;

a second insulating layer overlying portions of said second conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first conductive material layer and said second conductive layer pattern; and

a second conductive material layer filling said second plurality of contact holes, said second conductive material layer in contact with said first conductive material layer and said second conductive layer pattern.

67. The device of claim 66, wherein said conductive material layers comprise a metal.

G1 cont.

68. The device of claim 67, wherein said metal comprises tungsten.

69. The device of claim 66, wherein said first conductive layer pattern comprises a gate electrode.

70. The device of claim 66, wherein said first conductive layer pattern comprises a gate electrode overlying a gate oxide.

72. The device of claim 66, further comprising a junction layer on said substrate.

73. The device of claim 72, wherein said junction layer comprises a N+ junction layer.

74. The device of claim 72, wherein said junction layer comprises a P+ junction layer.

75. The device of claim 66, wherein said first conductive layer pattern comprises polysilicon.

76. The device of claim 66, wherein said first insulating layer comprises a first oxide layer.

77. The device of claim 66, wherein said first plurality of contact holes are formed by a photoresist process.

78. The device of claim 66, wherein said first plurality of contact holes are formed by a wet etch process.

G1 cont.

79. The device of claim 66, wherein said first plurality of contact holes are formed by a dry etch process.

80. The device of claim 72, wherein said first plurality of contact holes expose said junction layer.

82. The device of claim 66, wherein said first plurality of contact holes are filled by a CVD process.

83. The device of claim 66, wherein said second conductive layer pattern comprises polysilicon.

84. The device of claim 66, wherein said second insulating layer comprises a second oxide layer.

85. The device of claim 66, wherein said second plurality of contact holes are formed by a photoresist process.

86. The device of claim 66, wherein said second plurality of contact holes are formed by a wet etch process.

87. The device of claim 66, wherein said second plurality of contact holes are formed by a dry etch process.

88. The device of claim 66, wherein said second plurality of contact holes are filled by a CVD process.

G1 concluded